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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/002,461
Filing Date: November 01, 2001
Appellant(s): SLAVIN, KEITH R.

Edward L. Pencoske (Reg. # 29,688)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed November 18, 2008 appealing from the Office action mailed June 13, 2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

Claims 41-44 are allowed.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows: claims 41-44 are withdrawn from the 35 USC 112, 1st paragraph rejection. The rejection of claims 41-44 as being anticipated by Cheriton is withdrawn. Claims 4, 6-7, 11, 13-14,18, 20-21, 24 26-27 and 34-38 are withdrawn from the 35 USC 103 rejection of being unpatentable over Hariguchi et al. (P/N 6,665,297) in view of Cheriton (P/N 7,002,965).

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6665297	HARIGGUCHI et al.	12-2003
7002965	CHERITON	2-2006

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

35 USC 112, 1st Paragraph

The rejection of claims 1-38 under 35 USC § 112,1st paragraph is ***maintained*** and repeated below.

The following is a quotation of the first paragraph of 35 USC § 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-38 are rejected under 35 USC 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Delaying the input of the comparand word to the CAM has been claimed in claims 4, 11, 18 (17 in the office action was a typographical error), 24 and 34. A delay circuit is shown in

Figures 1 and 5, elements 28 and 114, respectively, however, nothing more than a blank box or a black box type design is depicted which fails to give any details for one of ordinary skill in the memory arts to make and use a delay circuit in conjunction with a content addressable memory without undue experimentation. The delay circuit is mentioned on page 4, paragraph 0019 and page 14, paragraph 0057 of the specification without providing sufficient technical details for essential subject matter. The claims state that the input word or comparand word is delayed in being input to the CAM until the enabling is completed, however, nothing is given which describes how a delay of the input is to be determined or what parameters must be met for a 'delay circuit' to be used. How does the determination of the enabling get performed and how is that determination used to notify the delay circuitry for the comparand word to be input to the CAM?

The written description does not detail how claimed aspects related to the delay circuit are to be made or performed. The law requires that the written description be clear and precise as to how the Applicant performs such activities as those claimed. If memory elements are not limited as to which types can be used and steps or instructions are not limited as to what step or instruction is performed, if the only 'teaching' is one or ordinary skill in the art already knows how to make and use, then where is the inventiveness of the present invention? The novelty of the present invention must be disclosed in such detail as to allow one of ordinary skill in the art to make and use the invention without undue experimentation. Such details for the actual inventive concepts have not been given in the present disclosure. Legal support for these reasons for a determination that the written disclosure is not adequate can be found in the recent

US Court of Appeals for the Federal Circuit, Automotive Technologies International, Inc., v. BMS of North America, Inc … (2006-1013,-1037).

35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5, 8-10, 12, 15-17, 19, 22-23, 25 and 28-33 are rejected under 35 USC 103(a) as being unpatentable over Hariguchi et al. (P/N 6,665,297) in view of Cheriton (P/N 7,002,965).

Hariguchi teaches the invention (claims 1, 8, 15, 22 and 28) as claimed including a method or circuit, the method or circuit comprising:

inputting an input word or comparand word with the word being Internet addresses which have different prefixes or indexes to a plurality of hash circuits, each hash circuit being responsive to a different portion of the input word as there being different hash circuits which are used dependent upon the prefix length with each hash circuit determining a match based upon a predetermined portion of the address (e.g., see Figures 2A-2B with support at col. 1, lines 23-50 and col. 5, lines 15-31);

outputting a hash signal from each hash circuit as each hash circuit (e.g., see elements *82-n* of Figure 2A) having an output to the selection stage (e.g., see element 88 of Figure 2A);

enabling or precharging portions of a CAM in response signals as portions of the CAM being enabled when an input is sent to the CAM (e.g., see col. 7, line 50 to col. 8, line 3);

inputting the input word or comparand word as inputting the input word (IP destination address) to the hash circuits and the CAM (e.g., see Figure 7, step 204);

comparing the input or comparand word (Internet address) in the CAM as identifying a hit from the comparison of the IP destination address and the contents of the CAM (e.g., see Figure 7);

outputting information responsive to the comparing of the input word (IP destination address) from either the hash circuits or the CAM (e.g., see Figure 7, steps 208 and 210);

a plurality of memory devices responsive to the hash circuits as hash buckets which respond to the entries of the hash stages and look-up tables (e.g., see Figures 2A-2B with support at col. 5, lines 15-63); and,

enable logic, responsive to the plurality of memory devices, for enabling portions of the CAM as being inherent as the CAM must have enable logic.

Hariguchi teaches the limitations of the independent claims as given above, however, the primary reference does not specifically teach using hash signals to enable portions of a CAM. Cheriton (P/N 7,002,965), the secondary reference teaches using a hash function to enable or choose portions of a CAM as generating classification indications which allows for packet classification in network routers (e.g., see Figure 3 with support at col. 6, line 43 to col. 7, line 21). It would have been obvious to one of ordinary skill in the memory arts at the time the invention was made to use hashing to select addresses in a CAM because using a CAM (or a TCAM) as a routing table or directory is a well known and common use of content addressable memories (e.g., see the background of Cheriton) and using hashing functionality for determining addresses for Internet address routing and address port information is also a common, well

known type of addressing. The combination of adding hash type addressing to using CAMs or TCAMs for routing data provides for a fast, methodical and reasonable use of current technology.

As to claims 2, 9, and 16, Hariguchi teaches assigning a mask to each hash circuit such that each hash circuit is responsive to a different n-bit portion of the input word or comparand word as different n-bit portions of the IP destination address being an associated prefix length of a predetermined portion of the address (e.g., see col. 5, lines 15-31).

As to claims 3, 10, 17 and 23, Hariguchi teaches inputting the least significant n bits of the input word or IP destination address to a memory and wherein the outputting selects between information responsive to finding a match of the address being found in the look-up tables or memory associated with the different hash circuits and the CAM (e.g., see Figure 2B with support at col. 5, lines 50-63).

As to claims 5, 12, 19 and 25, Hariguchi teaches enabling includes using the hash signals to select from a plurality of stored signals and using the selected stored signals to enable or precharge a portion of the CAM (e.g., see col. 4, line 63 to col. 5, line14).

As to claim 29, Hariguchi teaches the circuit is responsive to the hash signals includes a plurality of memory devices respond to the hash signals and enable logic for the plurality of memories with the memories being buffers, tables, registers and the CAM (e.g., see Figures 2A-2B).

As to claim 30, Hariguchi does not specifically teach using SRAMs for portions of the memory, however, the reference does teach using semiconductor memory including random access memory. Cheriton teaches using on-chip SRAM for the hash directory (e.g., see col. 6,

lines 43-65). It would have been obvious to one of ordinary skill in the memory arts to combine the teachings of Cheriton with the teachings of Hariguchi because both references use hash tables in the same manner with both references using semiconductor memory for this function. The present invention does not further define using SRAM for the hash circuitry over any other type of random access memory, therefore making it obvious to use SRAM as given in the secondary reference.

As to claim 31, Hariguchi teaches an output memory devices responsive to the CAM for outputting information in response to a match in the CAM as the selection stage (e.g., see Figure 2B with support at col. 5, lines 50-63).

As to claim 32, Hariguchi teaches an input memory device responsive to a portion of the comparand word and a switch responsive to the input memory device and the output memory device with the switch being inherent as part of the circuitry for the selection stage (e.g., see Figures 2A-2B).

As to claim 33, Hariguchi teaches having a processor (e.g., see Figures 2A-2B, element 54), the plurality of hash circuits as hash table having hash circuits with hash stages and hash bucket stages (e.g., see Figures 2A-2B, element 70) with the circuit response to the hash circuits receiving information from the processor (e.g., see Figures 2A-2B) as the information from the processor including router control procedures which uses the routing table (e.g., see Figures 2A-2B). Figure 4 also shows data and addresses from the CPU being input to the hash circuit and the hash bucket circuitry.

(10) Response to Argument

As to the arguments directed to the 35 USC112,1st paragraph rejection for an inadequate written description, the basis of this rejection is explained in the office action, however, claims 41-44 are removed from this rejection at this time.

The delay circuit appears to be very important to the operation of the present invention. There does not appear to be an embodiment in the present specification which does not require the delay circuit, however, there are several crucial details not given about the delay circuit. A delay circuit, per se, may be known in the art, however, the delay circuit of the present invention is used to delay the input of the input word to the CAM until the enabling of portions of the CAM has been completed. Nothing is given as to how this is accomplished. What allows the delay circuit to only activate when the enabling to the portions of the CAM has completed? There is not a clock signal shown which provides for a set amount of clock pulses to pass before the enabling takes place. This element appears to be more complicated than either the drawings or the description relates.

The rejection was given citing all of the claims, even though only dependent claims 4, 11, 18, 24 and 34 recite this element because there is not an embodiment in the present disclosure for not using the delay circuit. The delay circuit appears to be necessary for the enabling step of the use of the CAM in the independent claims, therefore, even though the independent claims do not have this element specifically cited, it appears to be necessary for the functionality of the present invention. Even though the present invention is not directed to '*some new type of delay circuit*' there still must be a complete enough description of this element for the delay circuit to be used in conjunction with the operation of the CAM which is specifically claimed. The delay circuit is

specifically claimed in no more detail than what is disclosed, as in the *Automotive Technologies International, Inc. v. BMS of North America, Inc.*, 501 F.3d 1274 (Fed. Cir. 2007). The delay circuit is essential subject matter as it is in the claims. Delay circuits may not be considered a *new field* of inventive endeavor, however, the delay circuit is used in a very specific way in the present invention without that usage being clearly described. As this application has not gone to the court, testimony for what would constitute a 'great deal of experimentation' is not applicable. Specific *evidence that a great deal of experimentation would be required to construct a delay circuit is not in the record in the instant application* is not applicable either.

As to arguments associated with claims 41-44, are moot as this rejection is withdrawn.

As to arguments associated with the hash signals being in parallel to the CAM (paragraph spanning pages 11-12 of the brief, section "C1"), the secondary reference, Cheriton teaches using the hash functions as an input to a CAM. The Cheriton reference specifically states the results of the hash directory match is used by one or more CAMs (see column 7, lines 7-12), thereby teaching enabling the CAM using the hash function output.

As to arguments of enabling or precharging a portion of the CAM in response to the hash output (first full paragraph on page 12 of the brief), a portion of the CAM can be either a subset of addresses in the CAM or the entire CAM. Cheriton teaches enabling at least a portion of the CAM at column 7, lines 9-10, where it is taught that the hash entry is used to generate "one or more classification indications" (where "one" classification indication at least reads on the claimed "portion"). In either condition, the CAM addresses are enabled in direct response to the output of the hash directory of the Cheriton reference.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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